

Notice of References CitedApplication/Control No.
09/388,766Applicant(s)/Patent Under
Reexamination
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2123

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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	U	IEEE Standard Multivalued Logic System for VHDL Model Interoperability (Std_logic_1164). Copyright 1993. ✓			
	V	Mueller, Martin. "Chronology TimingDesigner V1.2", Printed Circuit Design, San Francisco, CA. January 1993. ✓			
	W	Tzartzanis, Nestoras. "Verilog for Behavioral Modeling". February 3, 1998. Reprinted from www-scf.usc.edu/~ee577/tutorial/verilog/verilog_lec.pdf ✓			
	X	Silicon Integration Initiative, Inc. "Electronic Component Information eXchange (ECIX) – Timing Diagram Markup Language (TDML) Sample Instances". May 18, 1999. ✓			

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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